## REMARKS/ARGUMENTS

These remarks are made in response to the Office Action of May 30, 2007 (Office Action). As this response is timely filed within the 3-month shortened statutory period, no fee is believed due. However, the Examiner is expressly authorized to charge any deficiencies to Deposit Account No. 50-0951.

In the Office Action, claims 1, 3, 5-7, 9-11, 17, 19, 21-23, and 25-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,463,396 to Nishigaki (Nishigaki) in view of U.S. Patent No. 4,510,584 to Dias et al. (Dias). Claims 2, 8, 18, and 24 were rejected under 35 U.S.C. §103(a) as being unpatentable Nishigaki in view of Dias, and in further view of U.S. Patent Application No. 2002/0144163 to Goodfellow et al. (Goodfellow). Claims 4 and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable Nishigaki in view of Dias, and in further view of U.S. Patent No. 6,411,531 to Nork et al. (Nork) and U.S. Patent No. 6,633,494 to Roohparvar et al. (Roohparvar). Claims 12-14 and 30 were rejected under 35 U.S.C. §103(a) as being unpatentable under 35 U.S.C. §103(a) as being unpatentable Nishigaki in view of Dias, and in further view of non-patent literature "Switched-Capacitor DC-DC Converters for Low-Power On-Chip Applications" by Maksimovic et al. (Maksimovic).

### *Amendments to the Claims*

Although Applicant respectfully disagrees with the rejections asserted in the Office Action based on the cited references, Applicant has nonetheless amended the claims so as to expedite prosecution by further emphasizing certain aspects in the claims. Applicant respectfully asserts, however, that the amendments should not be interpreted as the surrender of any subject matter. Applicant is not conceding by these amendments that any previously submitted claims are not patentable over the references of record. Applicant's present claim amendments are only submitted for purposes of facilitating expeditious prosecution of the present Application. Accordingly, Applicant reserves the

right to pursue any previously submitted claims in one or more continuation and/or divisional patent applications.

In this response, Applicant has amended the claims to emphasize certain aspects of the claims. In particular, Applicant has amended independent Claims 1 and 17 to emphasize the operation and configuration of the claimed power supply integrated circuit (IC). For example, Claim 1 now recites the limitation that the DC to DC converter portion of the claimed IC includes structure for receiving a single DC supply voltage and for producing a plurality of output DC supply voltages. Furthermore, Claim 1 also now recites the limitation that the processing circuitry portion of the IC includes structure for receiving at least one of the DC supply voltages produced by the DC to DC converter portion of the claimed IC. Claim 1 also recites the limitation that the processing circuitry portion of the IC can modify at least one parameter of a received time-varying data signal. Additionally, Claim 1 has been amended to clarify that a produced time-varying data signal can be scaled to an output voltage level of one the DC supply voltages produced by the DC to DC converter portion of the claimed IC and received by the processing circuitry portion of the claimed IC. The limitations for the power supply IC in Claim 17 have been similarly amended with reference to other components in the claimed circuit board. Claim 17 has also been amended to clarify the interaction of the power supply IC to the other integrated circuits disposed on the claimed circuit board. Claims 2, 3, 18, and 19 have also been amended. All amendments in this response are fully supported throughout the Specification, as discussed below. No new matter has been added.

***Aspects of the Claims***

Prior to discussing the cited references, it may be useful to discuss certain aspects of the claims. The claims, as typified by Claim 1 recite a power supply IC (100), as shown in FIGs. 1 and 2 (reproduced below).

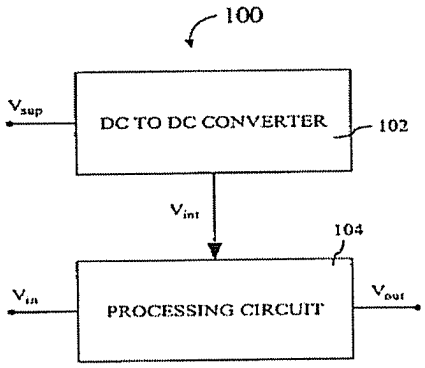


FIG. 1

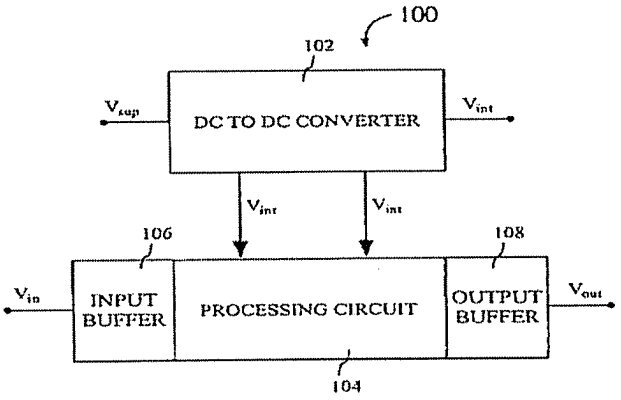


FIG. 2

The power supply IC (100) can receive a single DC supply voltage (Vsup) and at least one time-varying data signal (Vin), such as a radio frequency (RF) or microwave data signal. The power IC (100) comprises two portions, a DC to DC converter portion (102) and a translation or processing circuit (104) portion. The power supply IC (100) can produce from Vsup, using the DC to DC converter portion (102), a plurality of output DC supply voltages (Vint) which can be provided to power other ICs on a circuit board, as shown below in FIG. 3:

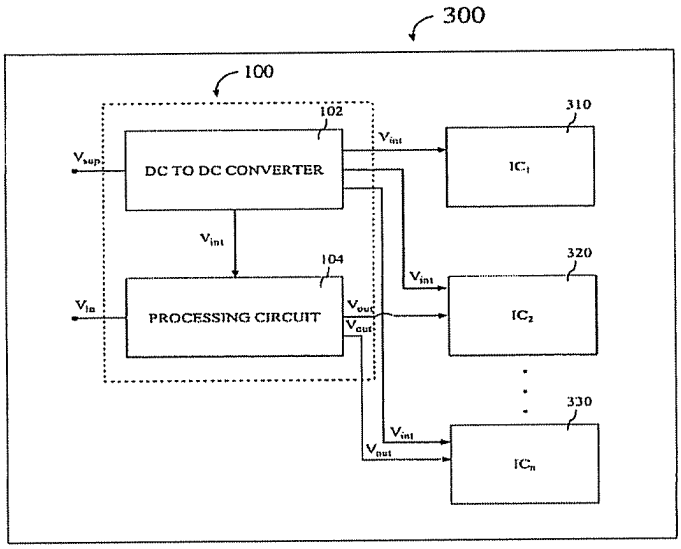


FIG. 3

At least one of the produced Vint can also be provided to the processing circuit portion of the IC (104), to provide power to operate the processing circuit portion (104), as shown in FIGs. 1-3. The processing circuit portion (104) can be used to modify at least one parameter of Vin (input time-varying data signal received by the IC), such as frequency, amplitude, or polarity, and produce at least one output time-varying data signal (Vout). (See, e.g., Specification, p. 16, lines 5-16, for polarity.) Vin and Vout inherently comprise a data signals, as Vsup and Vint are explicitly disclosed as the input and output supply voltages in the claims and the Specification. As noted, Vout can also be provided to other IC's on a circuit board (300). The processing circuit portion (104) further scales Vout according to a DC voltage level of at least one of Vint received by the processing circuit portion (104). For example, the Vint provided to IC2 in FIG. 3 can also be provided to the processing circuit (104) to provide the appropriate scaling required for IC2 to use Vout. Therefore, supply voltages for a plurality of IC's on a circuit board can be produced by a single IC, eliminating the need to include additional power supplies. Furthermore, the same IC can translate an input data signal into a one or more data signals usable by other IC's without having to provide multiple translation IC's.

***The Claims Define Over the Cited References***

In the Office Action, independent Claims 1 and 17 were rejected as being unpatentable over Nishigaki in view of Dias. Nishigaki discloses an apparatus for controlling internal heat generated for a computer system. Dias discloses a non-volatile random access memory cell. It is asserted in the Office Action that all the limiations of Claims 1 and 17, as previously submitted, were disclosed in Nishigaki and Dias. However, from the remarks in the Office Action, it is difficult to ascertain which limitation is disclosed, although it appears to be related to the operation of the processing circuit in the claims. Applicant therefore respectfully requests clarification of the use of

Dias against claims and 17. Nonetheless, Applicant submits that Nishigaki and Dias fail to disclose each and every element of the claims, as amended.

In particular, Nishigaki fails to disclose an integrated circuit in which only the DC to DC converter output is used to generate a supply voltage for the processing circuitry. In the Office Action, it is asserted that disclosed components PS1, PS2, and DS controller disclose the operation of the DC to DC converter and the processing circuit portions of the claimed IC. In particular, it is asserted that PS1 corresponds to the DC to DC converter portion and that PS2 and the DS controller correspond to the processing circuitry. Applicant respectfully disagrees. The construction and operation of the circuit disclosed in Nishigaki is very different from that recited for the IC recited in Claims 1 and 17.

First of all, the claims recite the limitation that the processing circuitry is powered solely by output supply voltages generated by the DC to DC converter. Although Nishigaki explicitly discloses in FIG. 3 that the P1 supply voltage, generated by PS1, is an input to the DS controller, nowhere does Nishigaki disclose or suggest that P1 is also an input for PS2. Rather, the input to PS2 is the same AC supply used as an input for PS1, as shown below in FIG. 4:

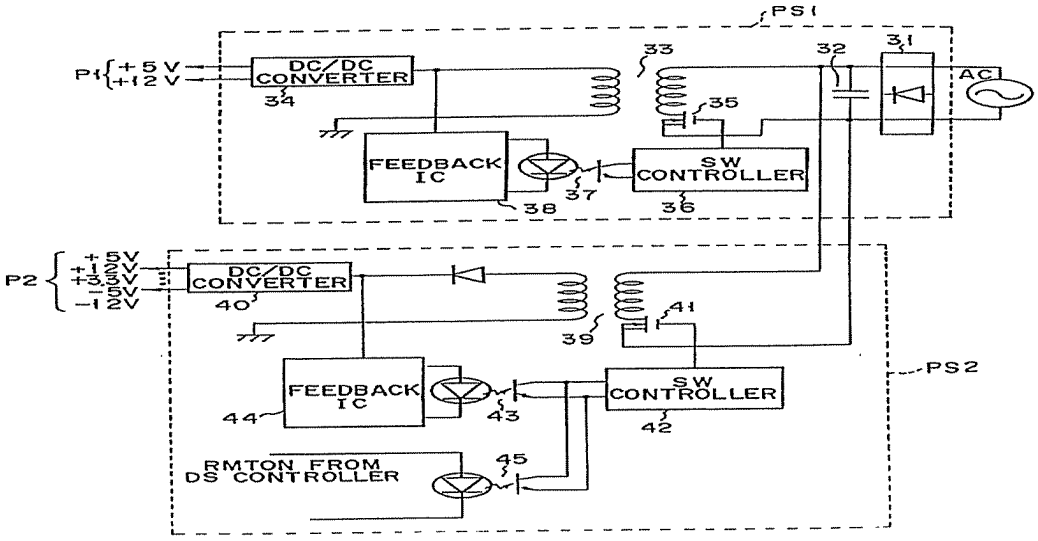


FIG. 4

Nowhere does Nishigaki disclose or suggest that one of the outputs of the DC/DC converter (34) of P1, as shown above in FIG. 4 could be routed or coupled to components in PS2 to generated the output voltages P2 generated by the DC/DC converter (40) of PS2. Rather, for each of DC/DC converters 34 and 40, a separate AC/DC converter 33, 39 is required to provide the appropriate input. In contrast, the claims recite the limitation that the power supply and the input signal (for scaling purposes) for the processing circuit portion of the claimed IC is provided and generated solely by the DC to DC converter portion of the claimed IC, not by an external AC source. Such a configuration is advantageous in that only a single DC supply is needed for the claimed IC, which in turn uses only a single DC supply to generate not only all the required supply voltages, but also all the required output signals.

Second of all, the claims recite the limitation that the processing circuit can be used to generate time-varying data signal. Nishigaki explicitly discloses in FIG. 3 that PS2 responds to inputs from the DS controller (RMTON signal). RMTON signal is generated in response to VCC signal variations. The RMTON signal is then used to modify the inputs into the SW controller (42) of PS2. Thus, Nishigaki does not disclose varying the input data signal VCC, but rather discloses varying the input supply AC signal for the rectifier in PS2. Furthermore, as shown in FIG. 4, P2 is not identified or used for providing a data signal, but rather is explicitly used as a power supply voltage for components 216 and 217. Additionally, PS2 discloses no method for scaling a signal in response to an output voltage level output through P1. Rather, Nishigaki simply provides an example in which the DC/DC converters 34, 40 happen to coincide, not that PS2 responds in any way to a voltage level output from PS1. RMTON also does not provide scaling, rather just an on/off signal for the rectifier, as the P2 voltages are used to supply power, not data signals. In contrast, the claims recite that Vin is a time-varying data signal used to generate other time varying data signals, not supply voltages. Such a configuration is needed in the claimed invention, as the purpose of the claimed IC is to

provided a "translated" data signal for various IC's which operate at different voltages, frequencies, polarities, or phases.

Finally, the claims recite the limitation that supply voltages and data signals are provided by a single integrated circuit. Although, Nishigaki discloses a circuit board having such components, it would be contrary to the teachings of Nishigaki to include such components in a single IC. Although Nishigaki does disclose that the DS controller components could all be included in an integrated circuit, nowhere does Nishigaki disclose or suggest that PS1 and PS2 would also be included. In contrast, because the claimed invention does not require the additional circuitry for producing two or more rectified AC signals, the various elements can be combined into a single integrated circuit, as one of ordinary skill in the art would recognize that an all-DC system could be integrated into a single integrated circuit as opposed to a system including an AC power supply.

Accordingly, Nishigaki and Dias, alone or in combination with any other reference of record, fail to disclose, suggest, or render obvious each and every element as recited in impendent Claims 1 and 17. Applicants, therefore submit that the independent claims define over the references of record. Furthermore, as the remaining claims depend from one of Claims 1 and 17, while reciting additional feature, the dependent claims likewise define over the reference of record.

## CONCLUSION

This application is now in full condition for allowance, which action is respectfully requested. Applicants request that the Examiner call the undersigned if clarification is needed on any matter within this Amendment, or if the Examiner believes a telephone interview would expedite the prosecution of the subject application to allowance.

Respectfully submitted,

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